Si3000SSI-EVB

EVALUATION BOARD FOR THE SI3000 WITH THE STANDARD SERIAL INTERFACE

Description

The Si3000SSI-EVB provides the modem system designer an easy way to evaluate the Si3000 solution.

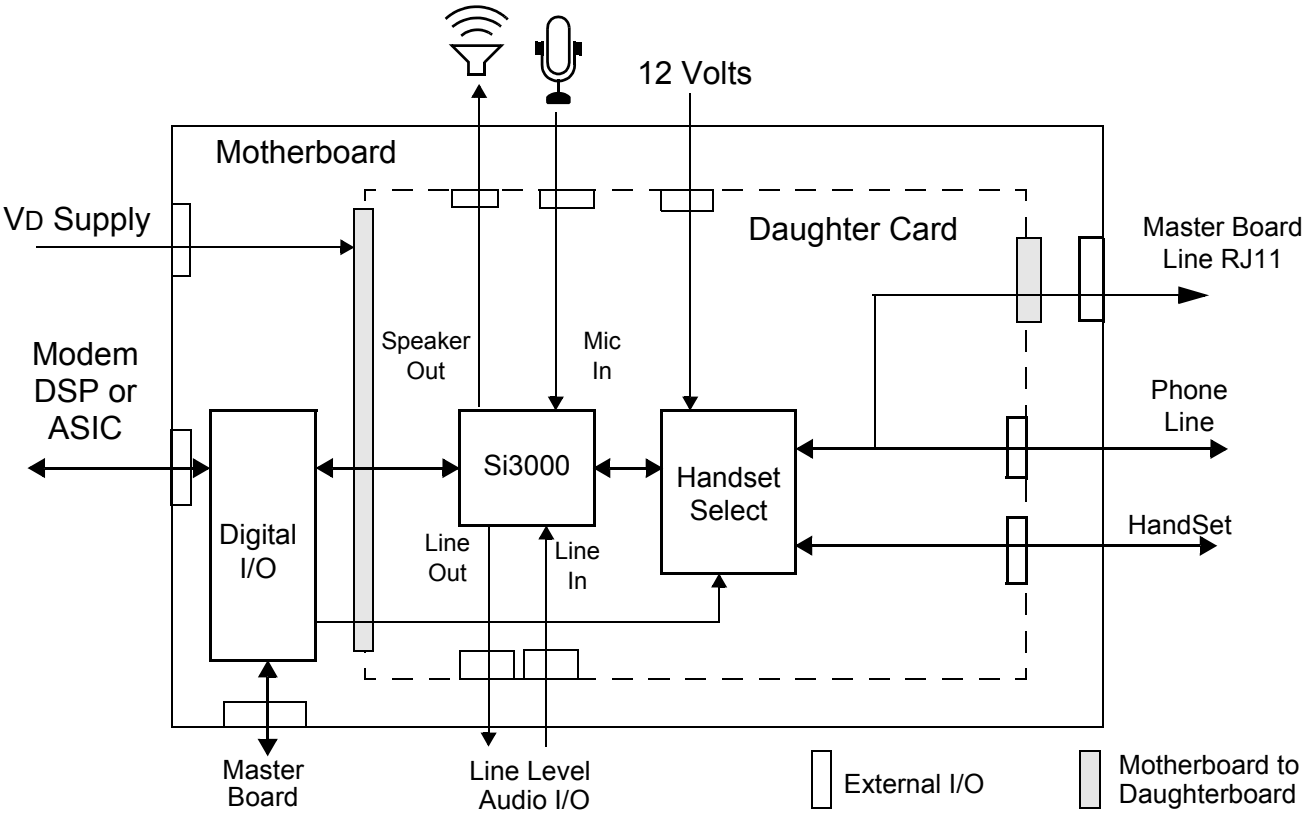
Power is supplied through two terminal blocks, V_D and V_A. This allows for 5-V or 3.3-V operation of the evaluation board.

Features

The Si3000SSI-EVB includes the following:

- RJ-11 Interface to Handset
- RJ-11 Connections to Phone Line and Modem
- Microphone, Speaker Interfaces
- Line In, Line out Interfaces
- Buffered Digital I/O Interface to DSP or ASIC
- Recommended Layout for Key Components
- Easy Power Connection for 5 V or 3.3 V Operation
- Easy Power Connection for Handset
- Flexible MCLK Scheme
- User Selectable Serial Mode
- Support for Daisy Chain Operation
- Motherboard–Daughter Card Connection

Function Block Diagram



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Functional Description

The Si3000SSI-EVB provides an easy way to evaluate the Si3000 solution.

This Si3000 device also supports the connection of multiple devices on a single serial interface. The evaluation board provides a straight forward means of evaluating this feature.

The evaluation board consists of the Si30xxSSI-EVB motherboard Figure 8/Figure 9 and the Si3000DC-EVB daughter card Figure 3/Figure 4. The Si30xxSSI-EVB can be used with other Silicon Laboratories daughter cards, such as the Si3034DC-EVB. Contact a Silicon Laboratories representative for more information.

In this document, the Si3000DC-EVB is occasionally referred to “daughter card”, and the Si30xxSSI-EVB as the “motherboard”. The Si3000SSI-EVB refers to the system which consists of both the “motherboard” and “daughter card.”

Motherboard–Daughter Card Connection

JP1 and JP2 on the daughter card are used to connect to the motherboard.

JP1 is a 3x8 socket connection to the digital signals of the Si3000. In addition, the V_D power of the motherboard (J2) is routed to this socket and supplies the power to the daughter card. JP1 connects to JP7 of the motherboard.

JP2 is a 2x5 socket connection to the Tip and Ring and chassis ground of the line interface to the handset selection circuitry. JP2 connects to JP8 of the Si30xxSSI-EVB.

Power Supply

Power is supplied to the Si3000SSI-EVB by means of J2, on the motherboard, when the board is used in stand-alone mode. If multiple boards are cascaded together, refer to the section on daisy-chain operation for the power supply requirements.

J2 is a euroblock header which allows for connection to a bench power supply. J2 provides the power for all devices connected to the V_D node.

J2 can nominally be 3.3 V or 5 V. Note that U3 and U4 can operate from either 3.3 V or 5 V. If Y1 is used, it must support 3.3 V operation if V_D = 3.3 V.

J3 is used to supply power to V_A. However, V_A is not used in conjunction with the Si3000DC-EVB.

Diodes D4 and D5 on the motherboard are used to protect the Si3000SSI-EVB against over-voltage or accidental terminal reversal. They are rated at 6.8 V.

Clock Generation

The Si3000 requires an MCLK input. The EVB provides two options for this requirement. MCLK can be provided via pin 1 of JP4 (on the motherboard) from the target system or from an oscillator installed in Y1 (on the motherboard). JP3 (on the motherboard) selects the MCLK source to the Si3000. In the Y1 position, the oscillator installed in Y1 is connected. If 3.3 V is the VD supply, Y1 must be a 3.3 V oscillator. In the JP4 position, the clock on JP4 is connected. Valid MCLK frequency ranges from 1 to 60 MHz.

If multiple boards are cascaded together, refer to the section on daisy-chain operation. Only the master board will need an MCLK from Y1 or JP4.

Optional Call Progress Speaker

This feature on the Si30xxSSI-EVB is used in conjunction with the Si3034/35 evaluation boards, but is not utilized by the Si3000.

Reset Circuit

The Si3000 requires an active low pulse on $\overline{\text{RESET}}$ following power up and whenever all registers need to be reset. Typically, the target system generates this signal and supplies it on pin 9 of JP4 (on the motherboard). For development purposes, the Si3000SSI-EVB includes a reset push button, SW1, that is a logic OR (active low) with the reset signal from the target system. U4 (of the motherboard) provides the reset logic and serves as a buffer. This circuit is not necessary in a production design.

If multiple EVBs are cascaded together, the reset signal should be generated by the master board. Using the SW1 pushbutton on slave boards will only reset that slave board and slave boards further down the chain.

Serial Modes

The Si3000 supports two different serial modes for a glueless interface to many standard DSP and ASIC serial ports. The serial mode of the Si3000 can be selected by JP1 and JP2 on the motherboard.

Table 1: Si3000 Serial Modes

M1	M0	Mode
GND	GND	FSYNC frames data
GND	V_D	FSYNC pulse starts data frame
V_D	GND	Slave Operation
V_D	V_D	Reserved

Several additional signals are required for proper operation of the serial interface. As mentioned in the clock generation section, an MCLK must be provided for the Si3000 to operate.

FSYNC, SCLK, SDI and SDO are also required signals to operate the Si3000. FSYNC provides the sychronization for the audio samples. This signal operates at the sample rate. A high to low transition marks the beginning of a new frame.

SCLK is an output of the Si3000 providing the bit clock for the audio samples. Data is valid on the falling edge of SCLK following a FSYNC start transition. SDI is audio samples to be transmitted and SDO is audio samples received.

The serial port signals are also used during a secondary frame to read and write the internal registers of the Si3000. Refer to the Si3000 data sheet for more details on internal registers and how to read and write those registers.

When using the board in stand-alone mode (single), set the motherboard switches as follows: SW2 = 1 and SW3 = 1. Figure 1 shows a typical configuration in stand-alone mode.

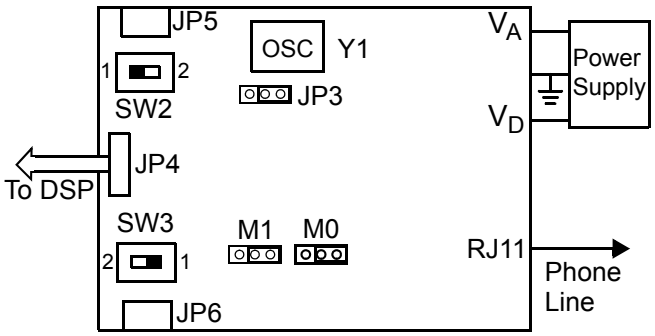


Figure 1. Stand-Alone Connections

Daisy-Chain Operation

The Si3000 supports an additional serial mode which places the device in a slave mode. This serial mode is accomplished by M1 = V_D and M0 = GND.

The Si3000SSI-EVB can essentially be used in two modes: stand-alone (single) and slave. Table 2 shows the configurations necessary for each mode.

Table 2: Si3000SSI-EVB Modes

Configuration	SW2	SW3	M1	M0
Single	1	1	GND	X
Slave	2	2	V_D	GND

In addition to JP1 and JP2 (which control the serial mode of the local Si3000), SW2 and SW3 are used to route the digital signals to ensure proper connection.

The SI3000SSI-EVB can be connected as a slave through JP6. Figure 2 shows the connection of a Si3034SSI-EVB as a master in daisy-chain mode. See the Si3034SSI-EVB data sheet for more details.

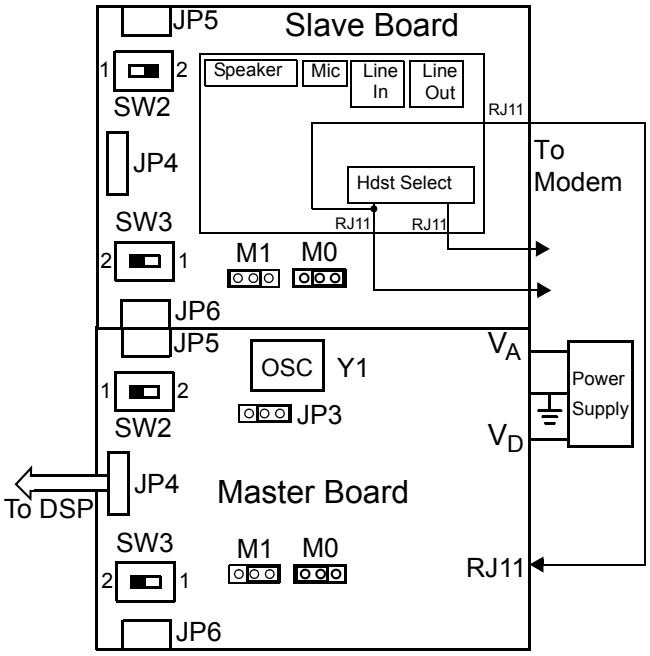


Figure 2. Daisy-Chain Connections

The DSP or ASIC target system connects directly to the master board. Only the master board needs a connection to a power supply. V_D is routed through JP5 and JP6.

When the Si3000SSI-EVB is used as a slave board, the serial mode must be M1 = V_D and M0 = GND. Be sure to configure SW2 and SW3 appropriately according to Table 2.

Line Connection

The Si3000SSI-EVB has two physical interfaces designed to connect to the phone line. One of the connectors is on the motherboard (Figure 8), J1 pins 3

and 4, while the other connector is on the daughter card (Figure 3). These interfaces are equivalent and interchangeable. When using the Si3000SSI-EVB in stand-alone mode, only one of these line interfaces is used.

When using the Si3000SSI-EVB in slave mode, one of the line interfaces is used to connect to the phone line, while the other line interface is used to connect to the Master Board Modem Line Interface. This way, both the Si3000SSI-EVB and Si3034SSI-EVB gain access to the phone line without requiring an external phone splitter.

Handset Interface

The Si3000SSI-EVB includes a handset interface. This interface is located on the daughter card J1 connector pins 9 and 10.

A handset can connect directly to the phone line or the the Si3000 device. The target system is expected to control the DPDT relay to select the handset connection. When the handset is connected to the Si3000, both the Si3000 and handset are disconnected from the phone line. In this case, the Si3000SSI-EVB supplies DC power to the handset through an external 12 VDC bench supply. The euroblock header, J6, on the daughter card is provided for this connection. 24.5 mA of DC loop current is supplied to the handset.

In a voice modem application, the Si3000SSI-EVB is configured in the slave mode, with an Si3034SSI-EVB acting as the master board. When this system is in the on-hook state, either the Si3034 or the handset can respond to the phone ring and place the system in the off-hook state.

If the system software chooses to allow the Si3034 EVB to go off hook, the handset is excluded from the phone loop and is connected directly to the Si3000 EVB. Voice traffic is handled by the Si3000 and system software is responsible for creating a virtual voice connection between the handset and the phone system through the Si3000 and Si3034 devices.

Microphone Interface

A standard 3.5 mm mini-phono connector located on the daughter card connector J2 is used to provide an interface from an external microphone to the Si3000. The input impedance to MIC input of the Si3000 is at least 10 kΩ. The Si3000 has a programmable pre-amplification to support many input line levels.

If Jumper JP3 on the daughter card is populated, the microphone can be powered directly from the Si3000 MBIAS output. The MBIAS output provides a typical voltage of 2.5 volts and can supply up to 5 mA, programmable through an external resistor. For applications that cannot be met by the Si3000's MBIAS output, the jumper may be removed and an external biasing voltage can be applied to the microphone.

Speaker Interface

A standard 3.5 mm mini-phone connector is located on the daughter card connector J3. The Si3000 SPKRR and SPKRL outputs are designed to drive 60 Ω loads directly. To drive a 32 Ω headset, an external series resistor (30 Ω) is needed. Driving a 32 Ω headset directly may result in reduced THD and Dynamic Range performance. The maximum voltage swing is 1 Vrms for either the left or right speaker drivers. The Si3000 speaker outputs have programmable analog attenuation.

Line Input Interface

A standard RCA jack on the daughter card connector J5 is used to provide the line-level audio inputs to the Si3000. The Si3000 has a programmable pre-amplifier. The input impedance of the LINEI is at least 10 kΩ. The Si3000 supports multiple levels of pre-amplification to support various line-levels.

Line Output Interface

A standard RCA jack on the daughter card connector J4 is used to provide the line-level audio outputs from the Si3000. The Si3000 line output gain is programmable. The maximum output voltage is 1 Vrms.

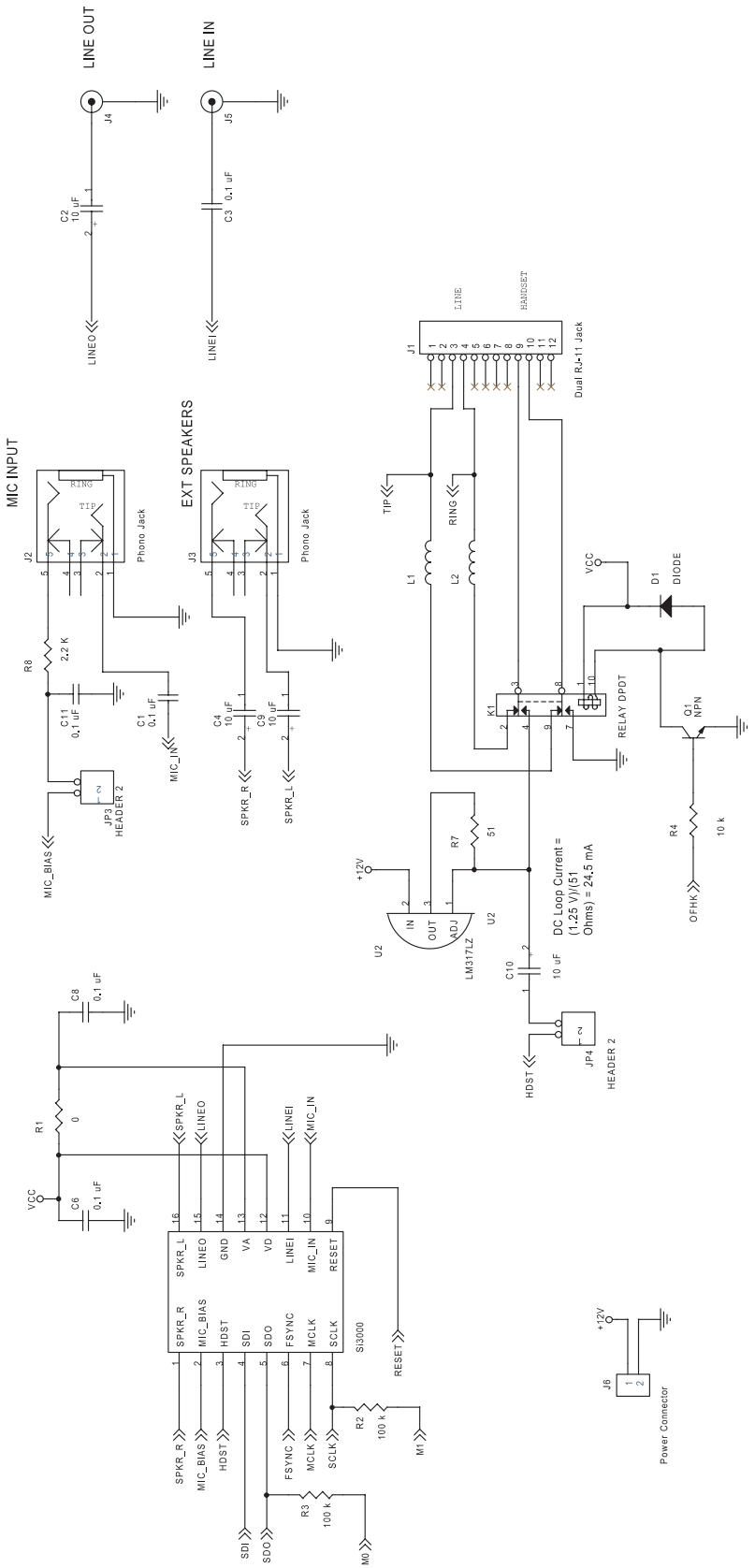
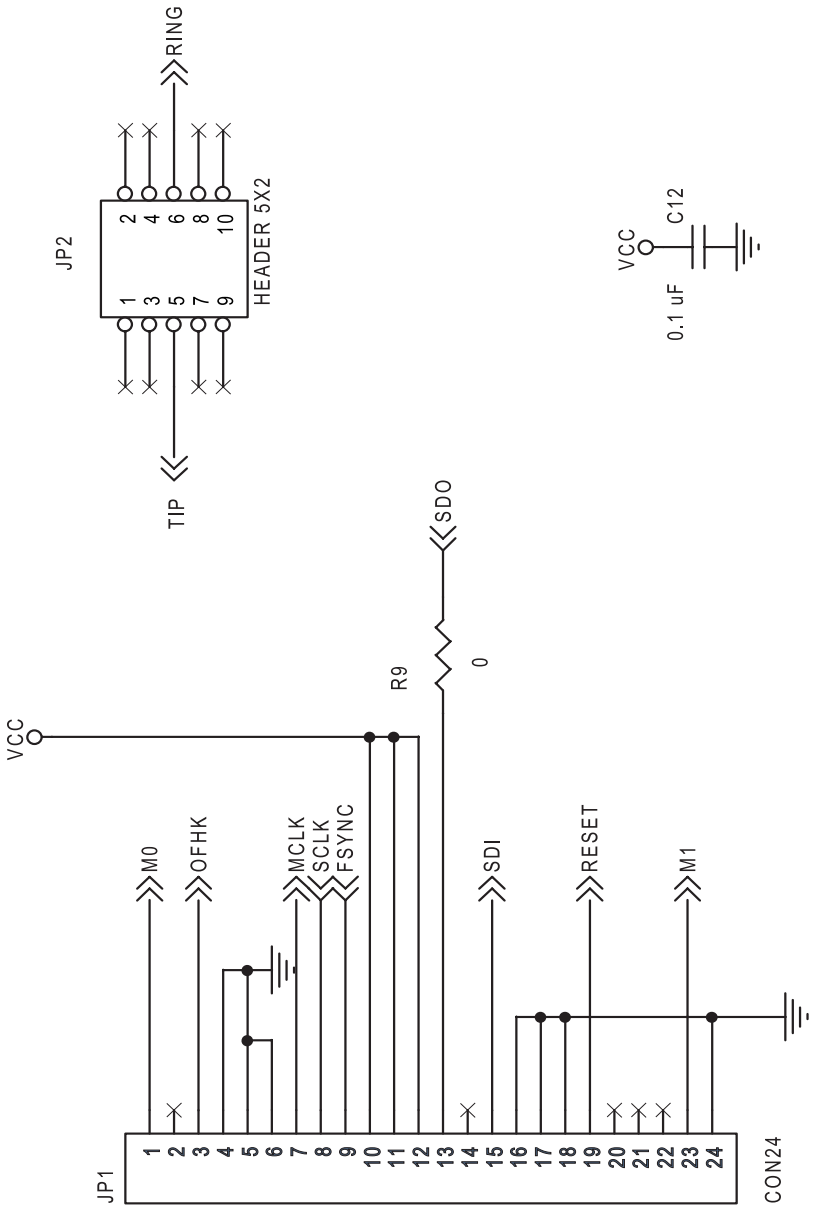
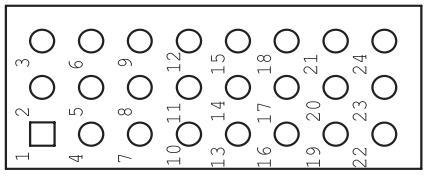


Figure 3. Si3000DC-EVB Schematic Page 1





Footprint of JP1
Top View

Figure 4. Si3000DC-EVB Schematic Page 2

Si3000DC-EVB Bill of Materials

Reference	Part
C1,C3,C6,C8,C11,C12	0.1 uF, 25 V, +/- 20%, 0805, X7R, C0805X7R250104-MNE, Venkel
C2,C4,C9	10 uF, 16 V, +/- 20%, case A, , TA016TCM106MAR, Venkel
C10	10 uF, 25 V, +/- 10%, case C, , TA025TCM106MCR, Venkel
D1	DIODE, , , DO-35, , 1N4148, Rectron
JP1	CON24, , , 3x8 100 mil, , SSW-108-01-T-T, Samtec
JP2	HEADER 5X2, , , 5x2 100 mil, , SSW-105-01-T-D, Samtec
JP4,JP3	HEADER 2, , , 2x1 100 mil, , 68000-402, Berg
J1	Dual RJ-11 Jack, , , RJ11x2, , MTJG-2-64-2-2-1, Adam Tech
J2,J3	Phono Jack, , , Thru-Hole, , 161-3504, Mouser
J5,J4	RCA JACK, , , thru-hole, , 16PJ097, Mouser
J6	Power Connector, , , thru-hole 2, , TSA-2, Adam Tech
K1	RELAY DPDT, 4.5V, , TQ2, , TQ2-4.5V, Aromat
L1,L2	Ferrite Bead, , , 1206, , BLM31A601S, MuRata
Q1	NPN, , , SOT-23, , CMPT2222A, Central Semiconductor
R9,R1	0, , , 0805, , CJ21-000-T, KOA
R3,R2	100 k, 1/10W, +/- 5%, 0805, , CR0805-10W-104JT, Venkel
R4	10 k, 1/4 W, +/- 5%, 1206, , CR1206-4W-103JT, Venkel
R7	51, 1/4 W, +/- 5%, 1206, , CR1206-4W-510JT, Venkel
R8	2.2 k, 1/10 W, +/- 5%, 0805, , CR0805-10W-222JT, Venkel
U1	Si3000, , , S016, , Si3000, Silicon Laboratories
U2	LM317LZ, , , TO-92, , LM317L, SGS Thompson

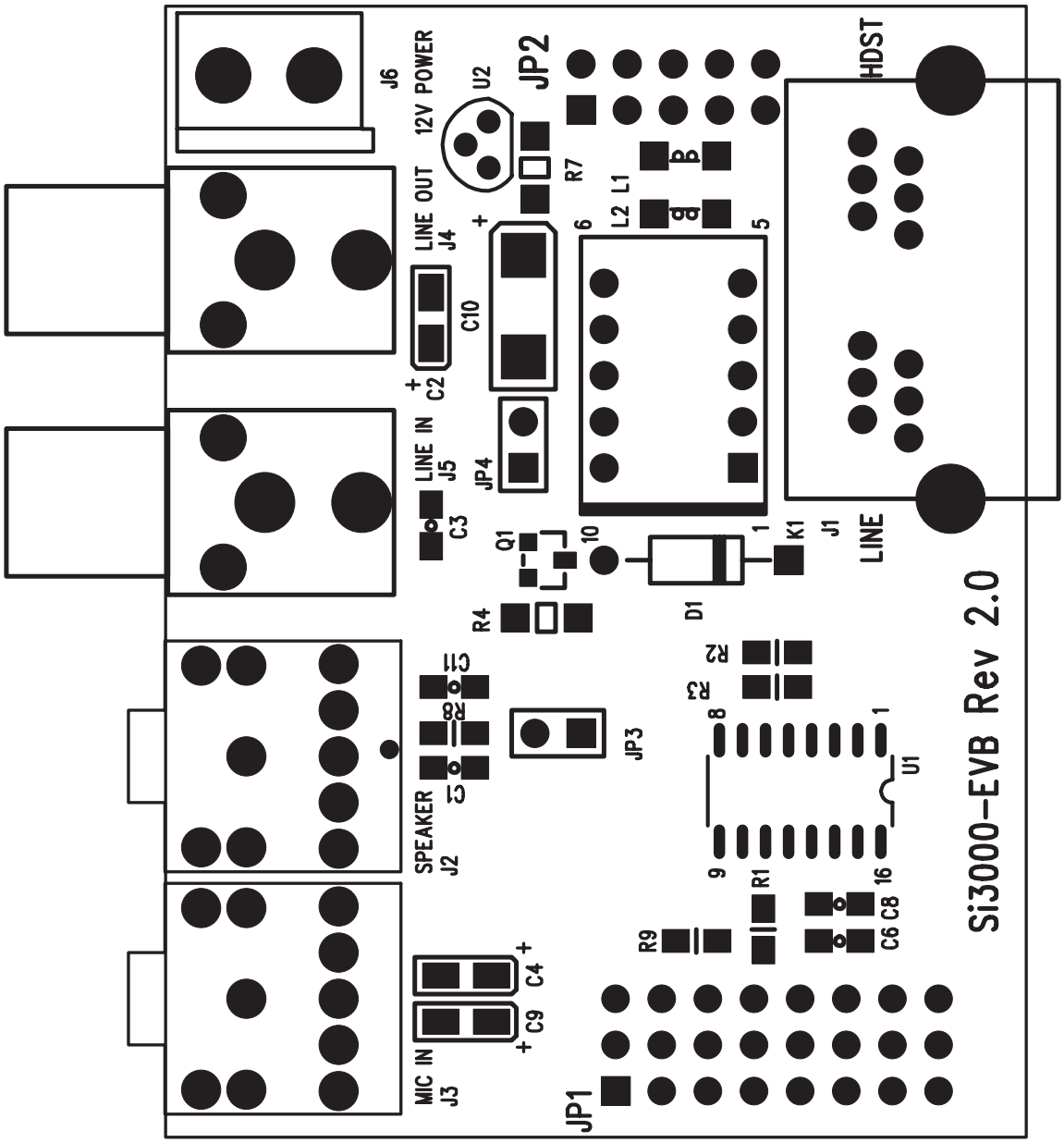


Figure 5. Si3000DC-EVB Silkscreen

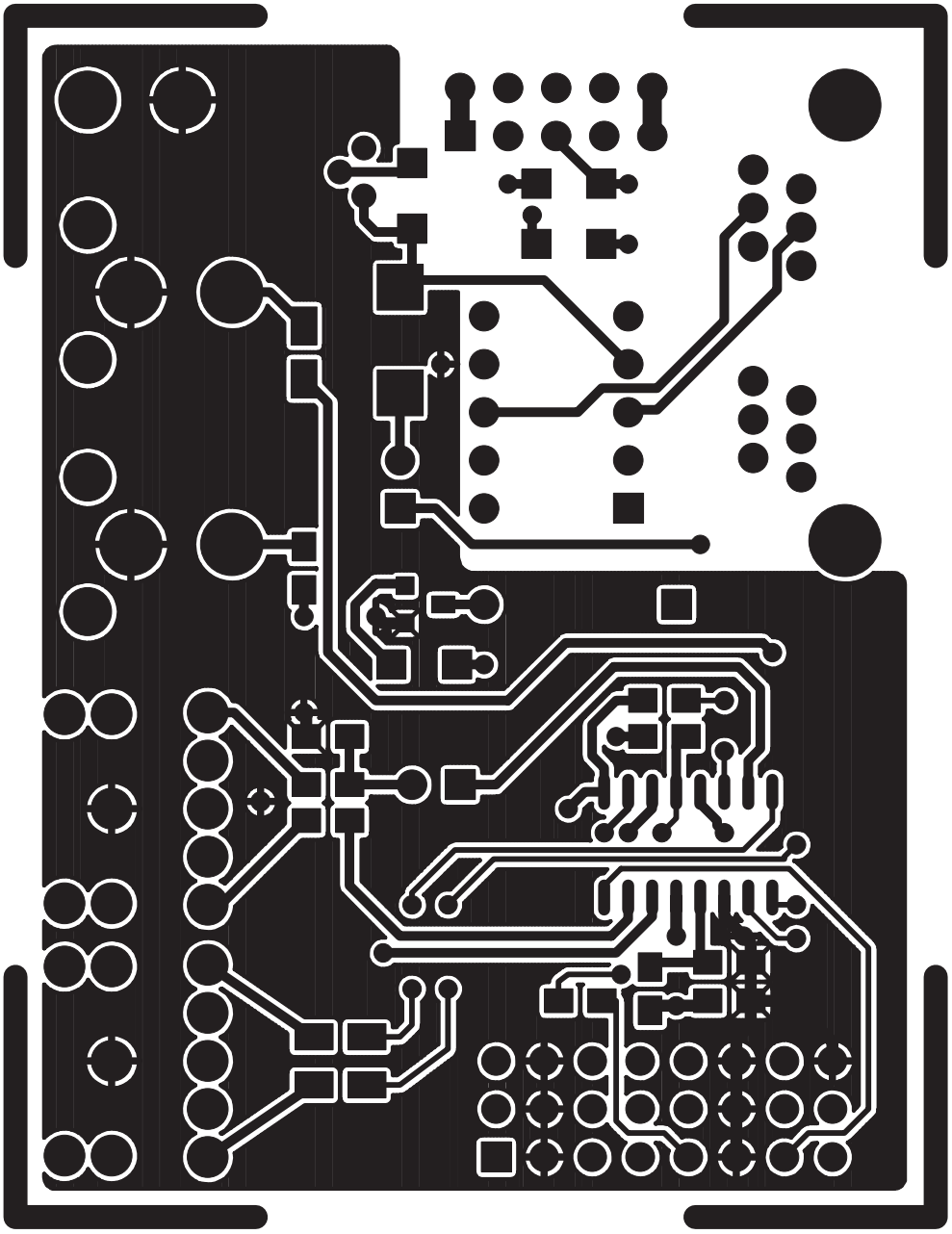


Figure 6. Si3000DC-EVB Component Side

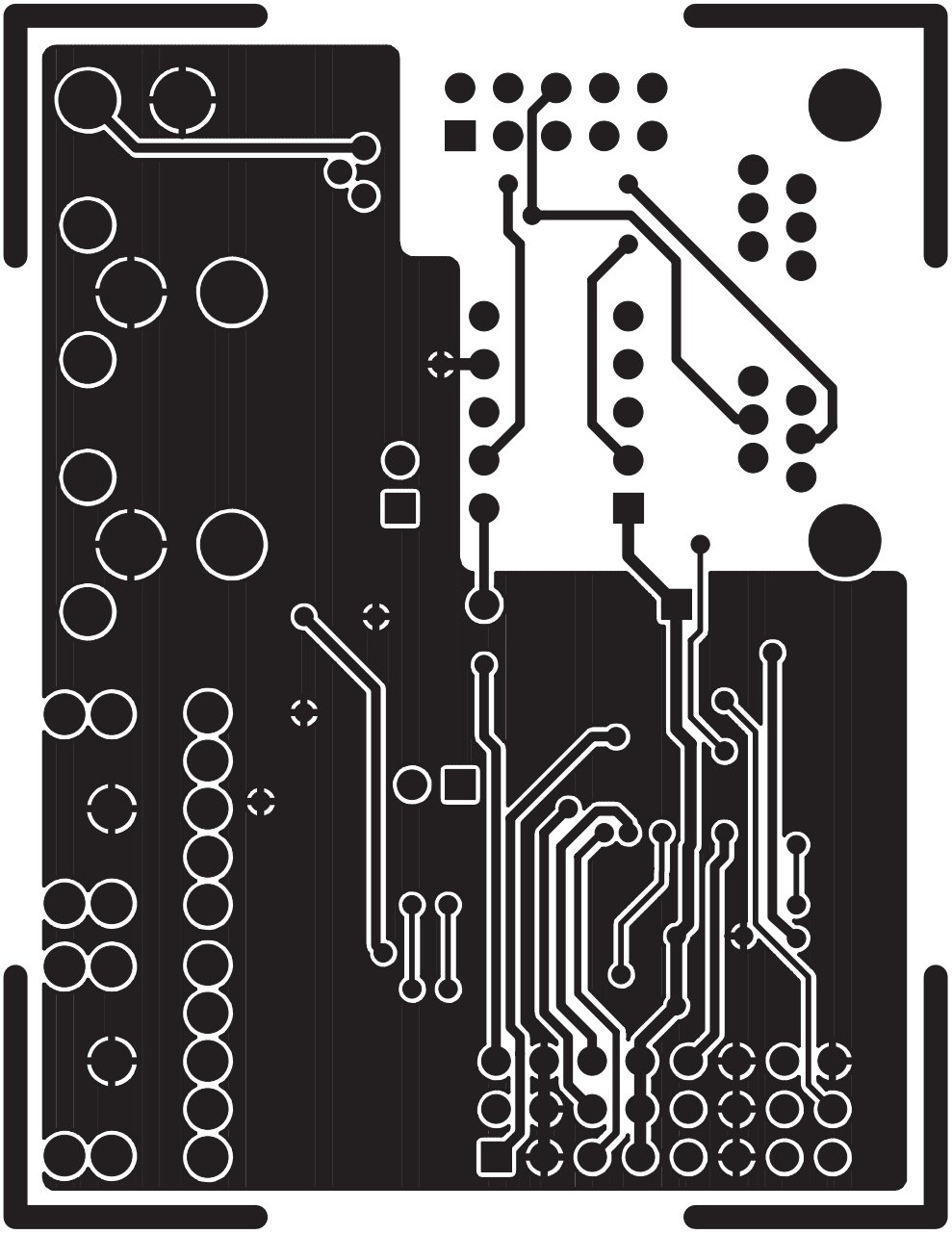
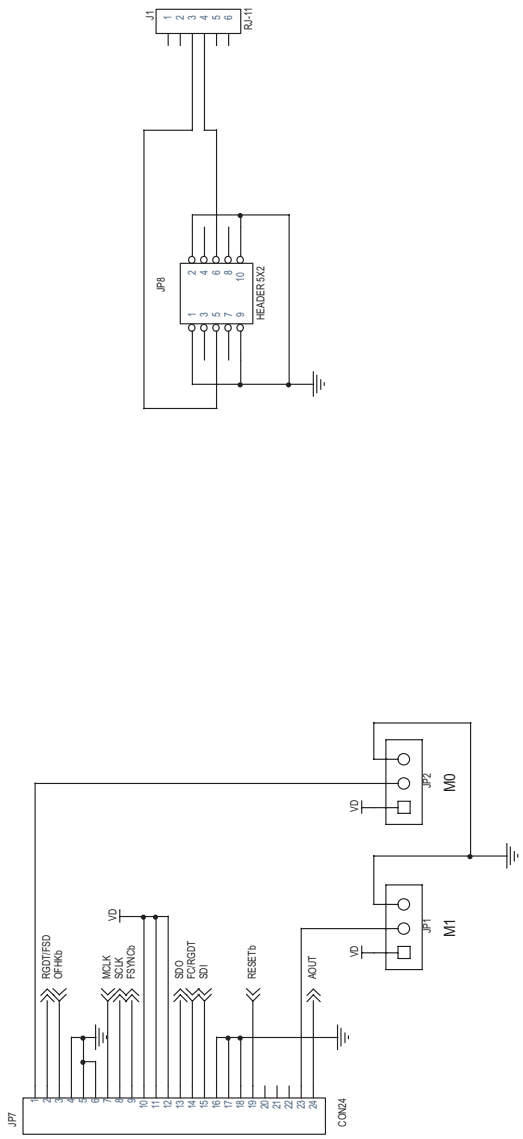
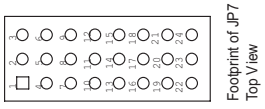


Figure 7. Si3000DC-EVB Solder Side





Footprint of JP7
Top View

Board Config.	SW2	SW3	M1	M0
Stand Alone	1	1	GND	X
Master w/ slaves	1	2	GND	VD
Slave	2	2	VD	GND

Figure 8. Si30xxSSI-EVB Schematic Page 1

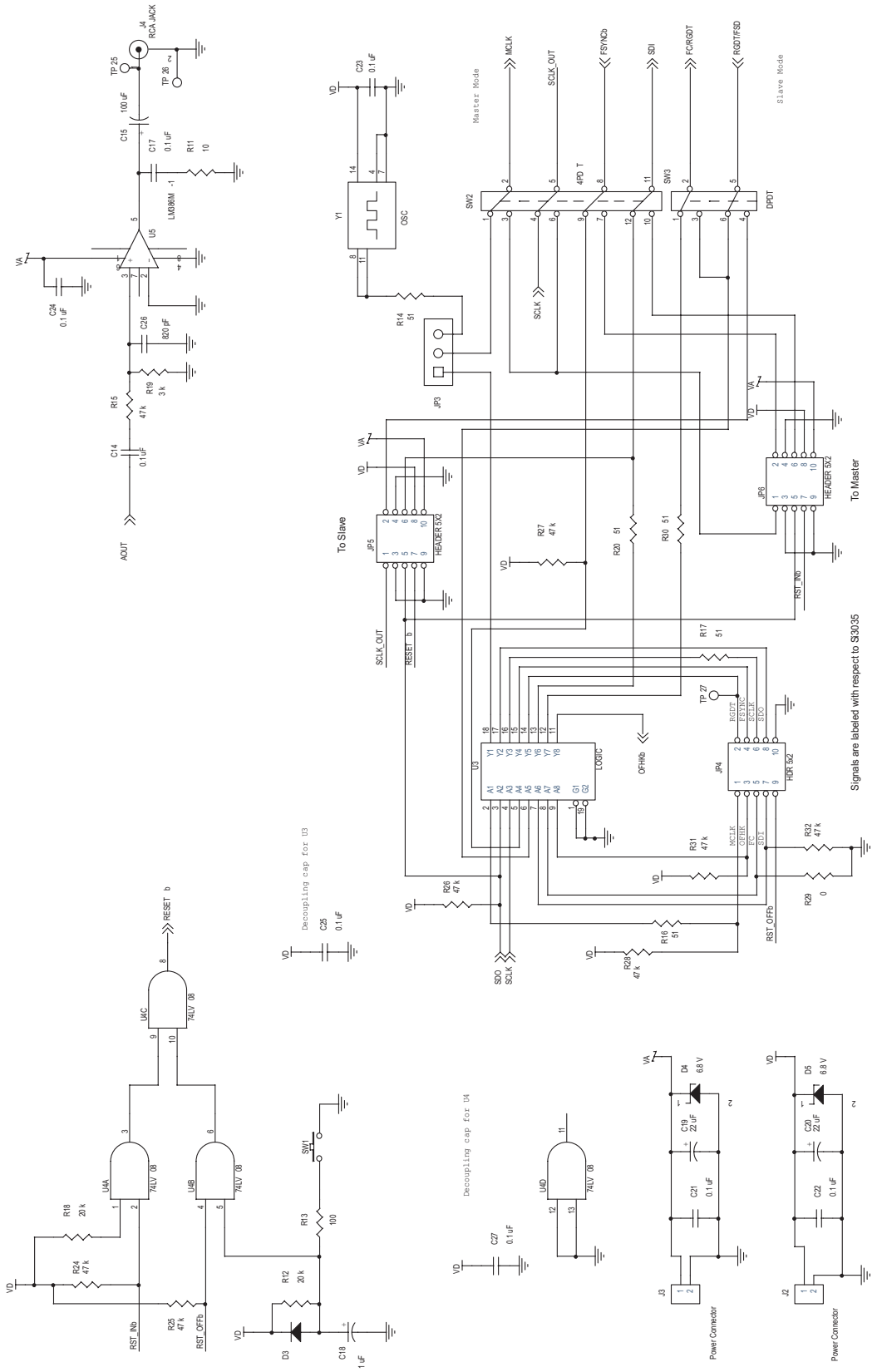


Figure 9. Si30xxSSI-EVB Schematic Page 2

Si30xxSSI-EVB Bill of Materials

Reference	Part
C14,C17,C21,C22,C23,C24, C25,C27	0.1 uF, 16 V, ±10%, 0603, X7R, C0603X7R160-104KNE, Venkel
C15	100 uF, 16 V, ±10%, case D, Tant, TA016TCM-107KDL, Venkel
C18	1 uF, 16 V, ±10%, case A, Tant, TA016TCM-105KAL, Venkel
C19,C20	22 uF, 16 V, ±10%, case B, Tant, TA016TCM-226KBL, Venkel
C26	820 pF, 50 V, ±5%, 0805, NPO, C0805COG500-821JNE, Venkel
D3	DIODE, 400 mA, 75 V, DO-35, , 1N4148, Diodes, Inc.
D4,D5	6.8 V, 6.8 V, , DO-15, , P6KE6.8A, Diodes, Inc.
JP1,JP2,JP3	3X1 Header, , , 3x1 100 mil, , 68000-403, Berg Electronics
JP4	HDR 5x2, , , 5x2 100 mil, , NSH-10DB-S1-T, Robinson-Nugent
JP5	HEADER 5X2, , , 10 pin thru-hole, , TSW-105-08-T-D-RA, Samtec
JP6	HEADER 5X2, , , 10 pin thru-hole, , SSW-105-02-T-D-RA, Samtec
JP7	CON24, , , 3x8 100 mil, , TSW-108-07-T-T, Samtec
JP8	HEADER 5X2, , , 5x2 100 mil, , TSW-105-07-T-D, Samtec
J1	RJ-11, , , thru-hole 6, , 154-0L6641, Mouser
J2,J3	Power Connector, , , thru-hole 2, , 506-5ULV02, Mouser
J4	RCA JACK, , , thru-hole, , 16J097, Mouser
R11	10, 1/10 W, ±1%, 0805, , NRC10F10R0TR, NIC Components
R18,R12	20 k, 1/10 W, ±1%, 0805, , NRC10F2002TR, NIC Components
R13	100, 1/4 W, ±1%, 1206, , MCR18EZHMFX1000, Rohm
R14,R16,R17,R20,R30	51, 1/10 W, ±5%, 0805, , CR21-510J-T, AVX
R15,R24,R25,R26,R27,R28, R31,R32	47 k, 1/10 W, ±5%, 0805, , NRC10J473TR, NIC Components
R19	3 k, 1/10 W, ±5%, 0805, , NRC10J302TR, NIC Components
R29	0, , , 0805, , CJ21-000-T, KOA
SW1	SW PUSHBUTTON, , , thru-hole 4, , 101-0161, Mouser
SW2	4PDT, , , SMT12, , ASE42L, Alcoswitch
SW3	DPDT, , , thru-hole 8, , ASE22L, Alcoswitch
TP25	Test Point, , , thru-hole, , 151-207, Mouser
TP26	Test Point, , , thru-hole, , 151-203, Mouser
TP27	Test Point, , , thru-hole, , 151-205, Mouser
U3	LOGIC, , , 20-pin SOIC, , CD74LPT541M, Harris
U4	74LV08, , , SO14, , 74LV08D, Philips
U5	OP-AMP, , , M, , LM386M-1, National Semi
Y1	OSC, , , DIP14, , ,

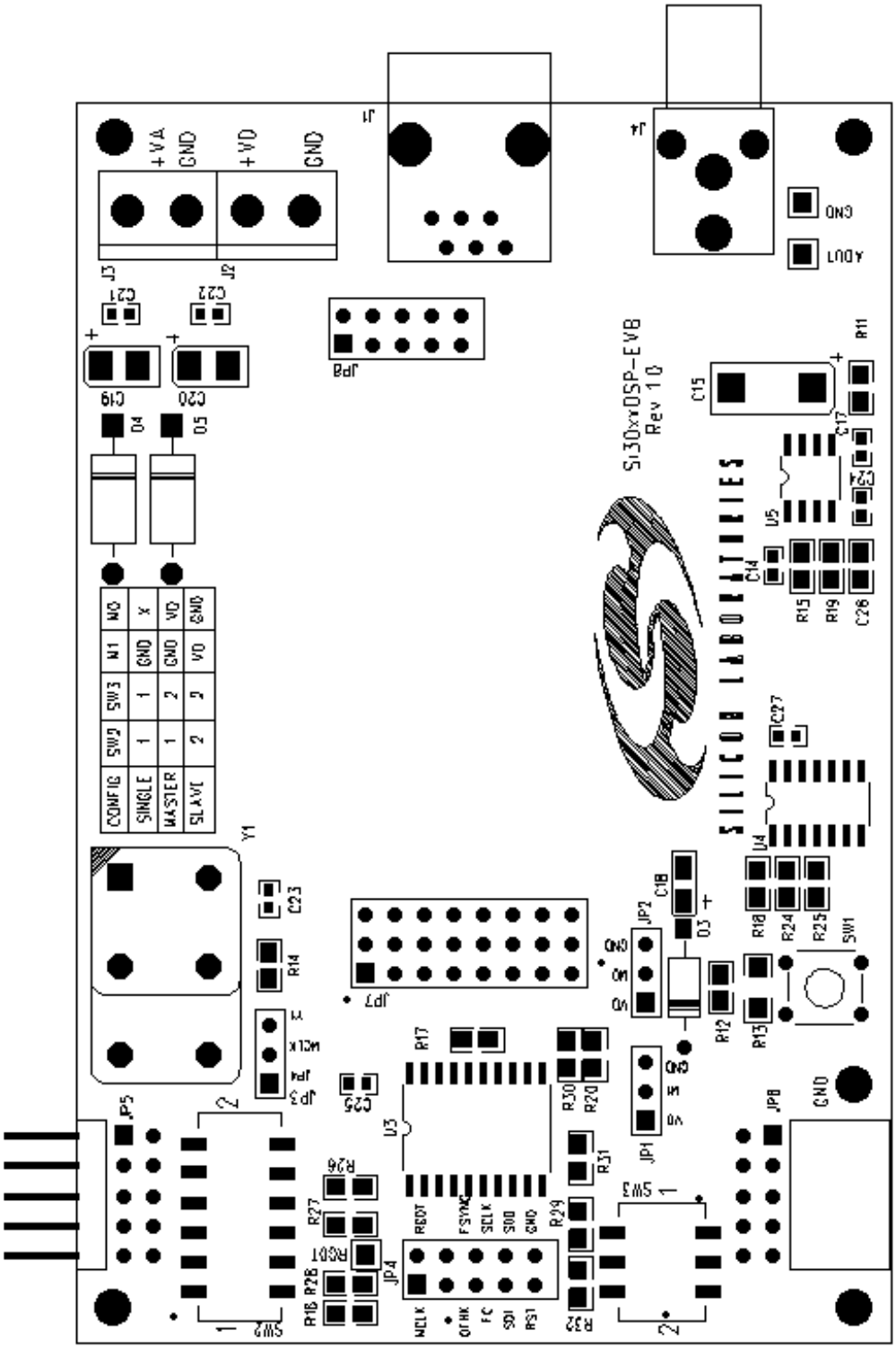


Figure 10. Si30xxSSI-EVB Silkscreen

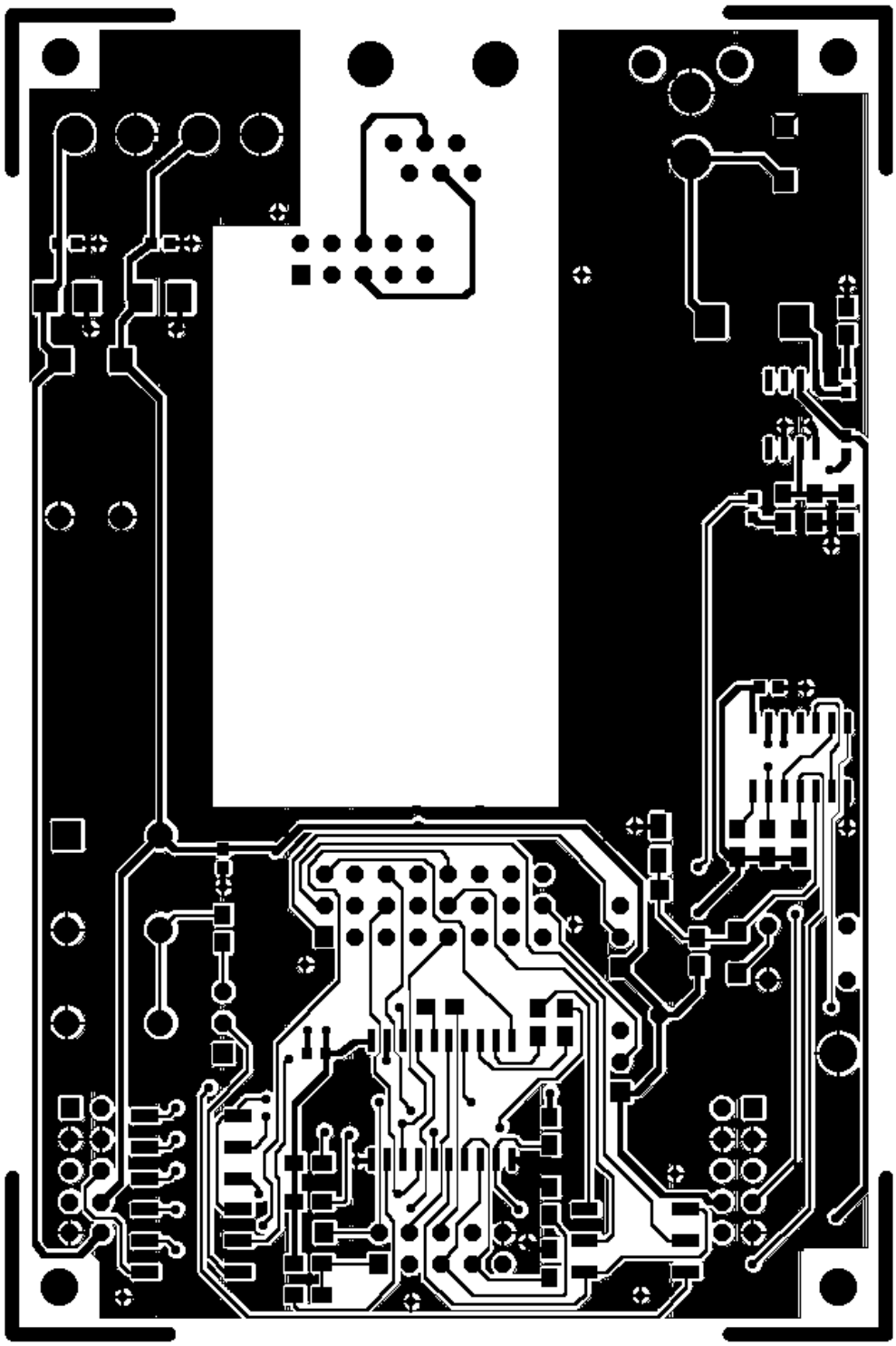


Figure 11. Si30xxSSI-EVB Component Side

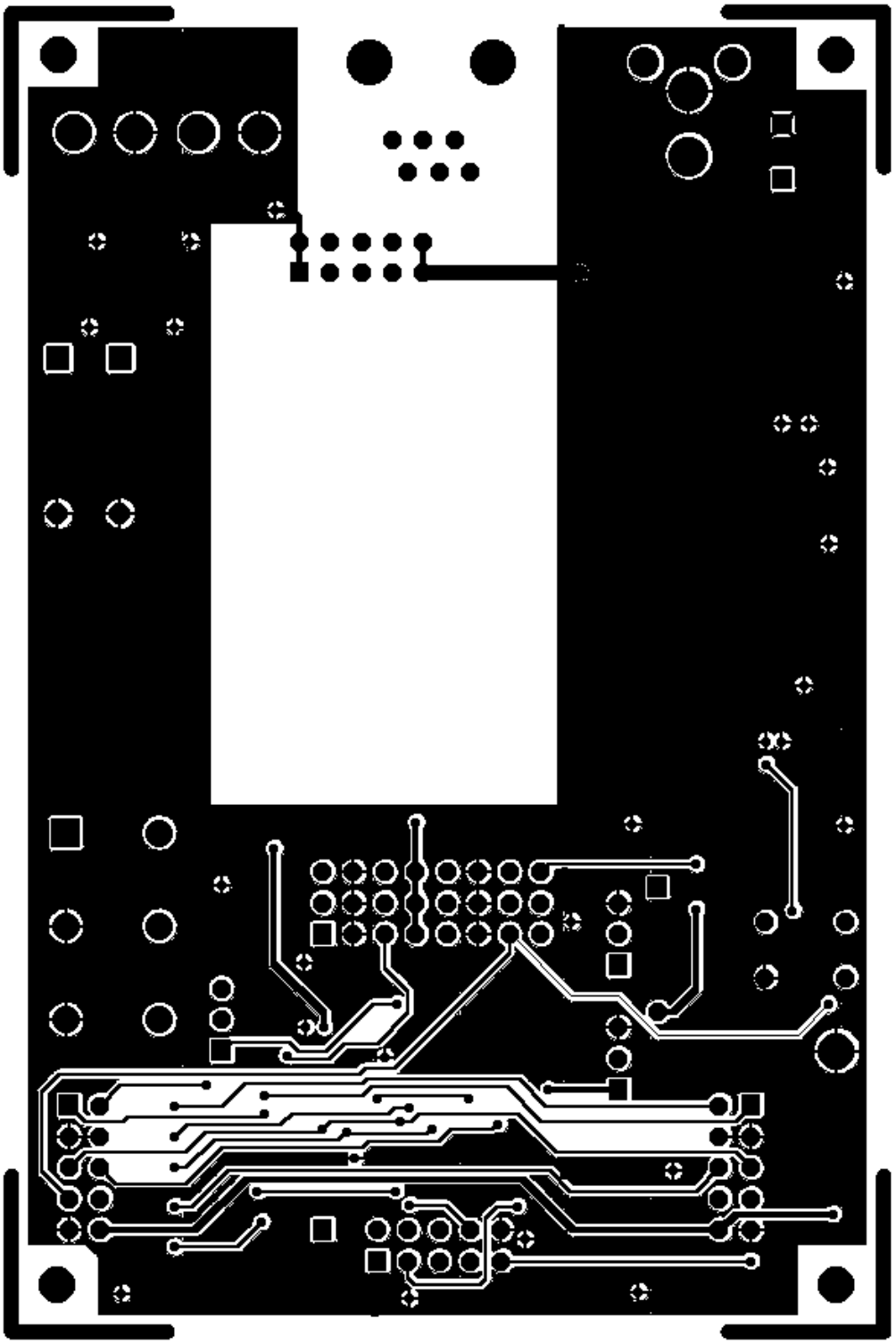


Figure 12. Si30xxSSI-EVB Solder Side

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